## Remarks

In the Office action dated May 9, 2005, the title of the application was objected to as non-descriptive, claim 4 was rejected as indefinite, and claims 1-4 and 6-8 were rejected as unpatentable over Chong et al. (US 6,727,151) in view of Nishida et al. (US Pub. No. 2003/0151098). In view of the forgoing amendments, the following remarks, and the Request for Continued Examination that is filed herewith, reconsideration and allowance of this application are respectfully requested.

As an initial matter, the title of the application has been amended to address the examiner's objection that it is non-descriptive. Therefore, this objection has been traversed.

Claim 4 has been cancelled without prejudice. Therefore, the rejection of claim 4 as indefinite has been traversed.

Amended claim 1 recites, *inter alia*, that a doped polysilicon sidewall is in direct contact with a pad oxide layer and a pad nitride layer. In contrast, Chong et al. disclose that second polysilicon spacers 26 forming lightly doped source/drain extensions are formed after the first polysilicon spacers 22 have been formed. Therefore, the doped polysilicon sidewall 26 is not in contact with the pad nitride 14.

Further, even though Nishida et al. disclose that a gate insulator (Fig. 13, DE) is formed within the opening, the gate insulator(DE) is not in contact with the pad oxide layer 12. Therefore, no combination of Chong et al. and Nishida et al. (the cited art) can render independent claim 1 or claims 2-3 and 6-8 obvious.

The cited art also fails to disclose using a polysilicon sidewall to form a gate electrode as recited in claim 1. Instead, Chong et al. disclose a method by which a source/drain is formed by the first polysilicon layer 22 having a gate electrode 36 formed therein. The remaining first polysilicon layer 22 itself serves as a source/drain region. In contrast to the structures disclosed by the cited art, the doped polysilicon sidewall recited in claim 1 does not act as a source/drain region but only as a mask for forming a source/drain region by, for example, doped ion implantations. In other words, the doped polysilicon sidewall determines the location of the gate electrode and, after forming the gate electrode, a source/drain region is formed.

The cited art also fails to disclose the LDD implantation structure recited in claim 1. Instead, Chong et al. disclose that first poly spacers 22 form the source/drain regions, and second poly spacers 26 form lightly doped source/drain extensions (column 3, lines 44-50). In addition, the channel of a transistor is formed at the epitaxial silicon layer 30, not the silicon substrate 10. In contrast, the source/drain region recited in claim 1 may be formed in the silicon substrate, in which case the doped polysilicon sidewall only determines the area forming the gate electrode. That is, the doped polysilicon sidewall is not the source/drain region itself. As a result, the pad oxide under the doped polysilicon sidewall acts as the LDD area thereby eliminating the need for a further LDD implantation process.

Therefore, none of the cited references or any combination thereof discloses or suggests all of the limitations recited by claim 1. Accordingly, independent claim 1 and claims 2-3 and 6-8 dependent thereon are in condition for allowance.

It is respectfully requested that the Examiner's rejections be withdrawn and that claims 1-3 and 6-8 be allowed. Reconsideration of this application and allowance thereof are respectfully requested. If there is any matter that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Respectfully submitted,

Hanley, Flight & Zimmerman
20 North Wacker Drive
Suite 4220
Chicago, Illinois 60606

Dated: 8.9.05

Mark G. Hanley
Reg. No. 44,736
Attorney for Applicant
312.580.1020